Course Title: Digital Logic (3 Cr.)
Course Code: CACS105
Year / Semester: I / I
Class Load: 5 Hrs. / Week (Theory: 3 Hrs. Practical: 2 Hrs.)

Course Description

This course presents an introduction to Digital logic techniques and its practical application in computer and digital system.

Course Objectives

The course has the following objectives:

- To perform conversion among different number system.
- To simplify logic functions.
- To design combinational and sequential logic circuit.
- To understand industrial application of logic system.
- To understand Digital IC analysis and its applications.
- Designing of programmable memory.

Course Detail

Specific Objectives	Course Content	Hours	References
• Explain the basic differences between digital and analog quantities. • Show how voltage levels are used to represent digital quantities. • Describe various parameters of a pulse waveform such as rise time, fall time, pulse width, frequency, period, and duty cycle. • Explain the basic logic functions of NOT, OR, and AND. • Describe several types of logic operations and explain their applications with example.	**Unit 1 : Introduction** 1.1 Digital Signals and Wave Forms 1.2 Digital Logic and Operation 1.3 Digital Computer and Integrated Circuits (IC) 1.4 Clock Wave Form	2 Hrs.	1. Chapter 1 - Introductory Concepts; Thomas L. Floyd, "Digital Fundamentals", 11th Edition," 2. Chapter 1 - Introductory Concept; Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems Principles and Applications", 10th Edition.

• Identify different types of digital integrated circuits according to their complexity and the type of circuit packaging. • Define clock wave. Explain terminologies related to Clock Wave Form.			
• Define Number system. Differentiate between positional and Non-positional number system with example. • Convert a number from one number system (decimal, binary, octal, hexadecimal) to its equivalent in one of the other number systems including both integer and floating type values. • Determine the 1's and 2's complements of a binary number. • Express signed binary numbers in sign magnitude, 1's complement, 2's complement, and floating-point format. • Apply arithmetic operations to binary numbers. • Carry out arithmetic operations with signed binary numbers. • Express decimal numbers in binary coded decimal (BCD) form. • Perform addition and subtraction operations on BCD numbers. • Explain the importance of the ASCII code. • Convert between the Binary System and the Gray Code and vice-versa. • Convert between the Binary System and the Excess – 3 Code and vice-versa. • Explain different types of Error Detection and Correcting Codes with their use.	**Unit 2 : Number System** 2.1 Binary, Octal & Hexadecimal Number Systems and their conversions 2.1.1 Representation of Signed Numbers, Floating Point Number 2.1.2 Binary Arithmetic 2.2 Representation of BCD, ASCII, Excess 3, Gray Code, Error Detection and Correcting Codes.	5 Hrs.	1. Chapter 2 – Number System, Operations, and Codes; Thomas L. Floyd, "Digital Fundamentals", 11th Edition," 2. Chapter 2 – Number Systems and Codes; Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems Principles and Applications", 10th Edition.
• Describe the operations of Basic, Universal, Ex – OR, and Ex – NOR gates with their functional expressions,	**Unit 3 : Combinational Logic Design** 3.1 Basic Logic Gates: NOT, OR and AND.	16 Hrs.	1. Chapter 3 – Logic Gates, Chapter 4 – Boolean Algebra and Logic Simplification, Chapter 5 –

Digital Symbol, Circuit Diagram, Truth table, Timing Diagram, and Venn diagram. • Realize the Universal Gates as Basic gates. • Define and apply the basic laws of Boolean algebra. • State and prove the DeMorgan's Theorem. • Explain the principle of Duality with example. • Simplify expressions by using the laws and rules of Boolean algebra. • Construct a truth table of Boolean expressions. • Define Canonical and Standard form of Boolean expression. • Convert any Boolean expression into Sum-Of-Product (SOP) form. • Convert any Boolean expression into Product-Of-Sum (POS) form. • Simplify the Boolean expressions using Karnaugh map method for both SOP and POS form including "Don't care" conditions. • Explain Combinational circuits with their features. • Implement digital logic for Half Adder, Full Adder, Half Subtractor, and Full Subtractor with their functional expression, logic diagram, truth table and timing diagram. • Explain the basic operations of encoders and decoders. • Design a logic circuit to decode any combination of bits. • Describe the basic Binary decoder. • Describe the BCD to Decimal decoder. • Use BCD-to-7-segment decoders in display systems. • Implement an octal to binary encoder. • Determine the logic for a decimal to BCD encoder. • Explain the purpose of the priority feature in encoders. • Describe decimal to BCD priority encoder. • Implement the 4 – bit Magnitude Comparator.	3.2 Universal Logic gates NOR and NAND. 3.3 Ex-OR and Ex-NOR Gates 3.4 Boolean Algebra: 3.3.1 Postulates & Theorems 3.3.2 Canonical Forms, Simplification of Logic Functions 3.5 Simplification of Logic Functions Using Karnaugh Map. 3.5.1 Analysis of SOP and POS expressions 3.6 Implementation of Combinational Logic Functions. 3.6.1 Half Adder and Full Adder 3.6.2 Encoders and Decoders 3.7 Implementation of data processing circuits. 3.7.1 Multiplexers and De-Multiplexers 3.7.2 Parallel Adder, Binary Adder, Parity Generator/Checker, and Implementation of Logic Functions using Multiplexers. 3.8 Basic Concepts of Programmable Logic 3.8.1 PROM 3.8.2 EPROM 3.8.3 PAL 3.8.4 PLA		Combinational Logic Analysis, Chapter 6 – Functions of Combinational Logic; Thomas L. Floyd, "Digital Fundamentals", 11th Edition," 2. Chapter 2 Boolean Algebra, Chapter 3 – Gate-Level Minimization, Chapter 4 – Combinational Logic, Chapter 7 – Memory and Programmable Logic; Morris Mano, "Digital Design", 5th Edition. 3. Chapter 3 – Describing Logic Circuits, Chapter 4 – Combinational Logic Circuits; Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems Principles and Applications", 10th Edition. 4. Chapter 9 – Programmable Logic Devices; Anil K. Maini, "Digital Electronics Principles, Devices and Applications", Wiley.

• Implement the 4 – bit parallel adder. • Describe the operation of basic parity generating and checking logic. • Explain the functioning of 9 – bit parity generator/checker. • Explain the basic operations of Multiplexers and Demultiplexers. • Explain the 4 line to 1 line, 8 line to 1 line and 16 line to 1 line multiplexers with logic diagram and truth table. • Implement the logic functions using the multiplexer. • Explain the functioning of 1 to 4 line Demultiplexer. • Explain the concept of programming logic with reference to PROM, EPROM, PAL and PLA with circuits and program tables.			
• Differentiate between latch and flip-flop. • Use logic gates to construct basic latches. • Differentiate between level triggering and edge triggering with their features. • Explain RS, JK, JK Master – Slave, D & T flip-flops with their logic diagram, graphical symbol, characteristic table, characteristic equation and excitation table. • Define resister. Identify the basic forms of data movement in shift resisters. • How SISO, SIPO, PISO and PIPO shift registers operate? Explain. • Define counter. Differentiate between Asynchronous and Synchronous counter. • Analyze the counter circuits and timing diagrams. • Explain the Ripple counter with Circuit, State, and Timing Diagram. • Explain the Ring counter with Circuit, State, and Timing Diagram.	**Unit 4 : Counter and Registers** 4.1 RS, JK, JK Master – Slave, D & T flip flops. 4.1.1 Level Triggering and Edge Triggering 4.1.2 Excitation Tables 4.2 Asynchronous and Synchronous Counters 4.2.1 Ripple Counter: Circuit, State Diagram, and Timing Wave Forms. 4.2.2 Ring Counter: Circuit, State Diagram, and Timing Wave Forms. 4.2.3 Modulus 10 Counter: Circuit, State Diagram, and Timing Wave Forms. 4.2.4 Modulus Counter (5, 7, 11) and Design Principles, Circuit and State Diagram.	16 Hrs.	1. Chapter 7 – latches, Flip-Flops, and Timers, Chapter 8 – Shift Registers, Chapter 9 – Counters; Thomas L. Floyd, "Digital Fundamentals", 11th Edition. 2. Chapter 5 – Synchronous Sequential Logic, Chapter 6 – Registers and Counters; Morris Mano, "Digital Design", 5th Edition. 3. Chapter 5 – Flip-Flop and related devices, Chapter 7 – Counters and Registers, Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, "Digital Systems Principles and Applications", 10th Edition. 4. Chapter 12 – Simple Digital Systems; Roger Tokheim, "Digital Electronics, Principles and Applications", 8th Edition, McGraw Hill.

• Explain Modulus Counter (5, 7, 10, and 11) with their Circuit and State diagram. • Describe the Synchronous counters: Binary Counter, Up-Down Counter, and BCD Counter with their circuit diagrams and state diagrams. • Construct the logic circuit diagram for Digital Watch and Frequency counter.	4.2.5 Synchronous Design of Above Counters, Circuits Diagrams and State Diagram. 4.3 Application of Counters 4.3.1 Digital Watch 4.3.2 Frequency Diagram 4.4 Registers 4.4.1 Serial in Parallel out Register 4.4.2 Serial in Serial out Register 4.4.3 Parallel in Serial out Register 4.4.4 Parallel in Parallel out Register 4.4.5 Right Shift, Left Shift Register		
• Define Finite state machine with example. • Explain the Mealy and Moore models of Finite State Machines. • Describe the State, State Diagram and State Table of Sequential Circuit. • Apply the State reduction through partitioning method to implement sequential circuit. • Describe the design procedure for sequential machines. • Use the flip – flops to realize the sequential machines. • Construct the Counters.	**Unit 5 : Sequential Logic Design** 5.1 Basic Models of Sequential Machines • Concept of State • State Diagram 5.2 State Reduction through Partitioning and implementation of Synchronous Sequential Circuits. 5.3 Use of flip flops in realizing the models 5.4 Counter Design	6 Hrs.	1. Chapter 5 – Synchronous Sequential Logic; Morris Mano, "Digital Design", 5th Edition.

Teaching Methods

The general teaching methods includes class lectures, group discussions, case studies, guest lectures, research work, project work, assignments(theoretical and practical), and exams, depending upon the nature of the topics. The teaching faculty will determine the choice of teaching pedagogy as per the need of the topics.

Evaluation

Evaluation Scheme				
Internal Assessment		External Assessment		Total
Theory	Practical	Theory	Practical	100
20	20 (3 Hrs.)	60 (3 Hrs.)	-	

Internal/Practical Assessment Format [FM = 40]

Internal Assessment Format [FM = 20] – Subject Teacher				
Term Examination		Assignment	Attendance	Total
Mid - Term	Pre - Final			
5	5	5	5	20

Practical Assessment Format [FM = 20] – External Examiner will be assigned by Dean Office, FOHSS.			
Practical	Viva	Lab Reports	Total
10	5	5	20

Note: Assignment may be subject specific case study, seminar paper preparation, report writing, project work, research work, presentation, problem solving etc.

Final Examination Questions Format [FM = 60, PM = 24, Time = 3 Hrs.]

SN	Question Type	Number of Questions Given	Marks per Question	Total Marks
1	Group – 'A' Objective Type Questions(Multiple Choice Questions)	10	1	10 x 1 = 10
2	Group – 'B' Short Questions (Attempt any SIX questions)	7	5	6 x 5 = 30
3	Group – 'C' Long Questions (Attempt any TWO questions)	3	10	2 x 10 = 20

- Student must pass 'Internal Assessment', 'Practical Assessment' and 'Final Examination' separately.
- Student must attend each and every activity of 'Internal Assessment' otherwise he/she will be declared as 'Not Qualified' for final Examination.

<u>Text Books</u>

1 Floyd, "Digital Fundamentals", PHI.
2 Morris Mano, "Digital Design", PHI,
3 Tocci, R. J., "Digital Systems – Principles & Applications", PHI

Reference Books

1 B. R Gupta and V. Singhal, "Digital Electronics", S.K. Kataria & Sons, India.
2 Fletcher, W. I., "An Engineering approach to Digital Design", PHI.
3 Millman & HalKias, "Integrated Electronics".
4 V.K. Puri, "Digital Electronics", Tata McGraw Hill.

Internal Assessment marks Submission format

Campus Name:									
Subject Name: Digital Logic						**Subject Code: CACS105**			
SN	**TU Registration No.**	**Name**	**Symbol No.**	**Mid – Term [5]**	**Pre – Final [5]**	**Assignment [5]**	**Attendance [5]**	**Total [20]**	**Remarks**

Name of Subject Teacher:

Signature:

Date:

Name of Director/HoD/Coordinator:

Signature:

Date:

Tribhuvan University

Bachelor in Computer Application (BCA) - 1st Semester

Digital Logic (CACS105)

Laboratory Report format

1. **Title:**

2. **Objectives:**

3. **Apparatus:**

4. **Theory:**

    Introduction

    Functional Expression

    Circuit Diagram

    Truth Table

    (You can add more topics here as per the nature of experiment)

5. **Procedure:**

6. **Result:**

7. **Remarks:**

Laboratory Activities

1. Implement any Basic Integrated Circuit(IC) to define the nomenclature of IC, Data sheet, concept of: power supply, input pins, output pins, V_{cc}, ground, IC Base and project board.
2. Implement Basic Gates, AND, OR and NOT.
3. Implement Universal Gates, NAND and NOR gates.
4. Verify the functioning of Exclusive - OR and Exclusive – NOR gates.
5. Realize the Basic gates using NAND gate.
6. Realize the Basic gates using NOR gate.
7. Prove the DeMorgan's Theorem using gates.
8. Implement the given Boolean function using logic gates in both SOP and POS forms.
9. Implement both half and full Adders using gates.
10. Implement both half and full Subtractors using gates.
11. Verify the functioning of 4-bit binary parallel adder.
12. Implement the Octal to Binary encoder.
13. Verify the operations of Decimal to BCD Encoder.
14. Verify the operations of 3 - to - 8 line Decoder.
15. Implement the BCD to Decimal Decoder.
16. Implement the BCD to 7 – Segment display Decoder.
17. Implement 16:1 Multiplexer.
18. Implement 1:16 Demultiplexer.
19. Verify the functioning of Flip flops (i) RS, (ii) JK, (iii) JK Master – Slave, (iv) D, and (v) T.
20. Show the operations of a 3-bit synchronous binary counter.
21. Show the operations of a 3-bit Asynchronous binary counter.
22. Design the mod - 10 counter.
23. Verify the functioning of Shift Registers, (i) SISO, (ii) SIPO, (iii) PISO, and (iv) PIPO.
24. Design Digital watch by Counters.
25. Design frequency counter.

Dear Teachers, it's only a guideline for lab work in Digital Logic, apart this you can add more activities in laboratory to make clear in applications of the course.

SET - A

Tribhuvan University

Faculty of Humanities & Social Sciences

OFFICE OF THE DEAN

2018

Bachelor in Computer Applications	**Full Marks: 60**
Course Title: Digital Logic	**Pass Marks: 24**
Code No: CACS 105	**Time: 3 hours**
Semester: I^st^	

Centre: **Symbol No:**

Candidates are required to answer the questions in their own words as far as possible.

Group A

Attempt all the questions. **10×1 = 10**

Circle (O) the correct answer.

1. The gray code 1111 is equivalent to binary is,

   a) 1001 b) 1010

   c) 1000 d) 1100

2. What is the input of a de-multiplexer, which has 3 selection bits.

   a) 8 b) 4

   c) 1 d) 6

3. To find .... of an algebraic expression we simplify interchange OR and AND operators and replace 1's by 0's and 0's by 1's.

   a) Complement b) Dual

   c) Canonical form d) De Morgan's

4. The result of binary subtraction 110001011 – 11101101 is,

   a) 10010110 b) 10100110

   c) 101101110 d) 10011110

5. The bit capacity of a memory that has 10 bit address input and can store 8 bits at each address is,

   a) 80 b) 8192

   c) 800 d) 1024

6. The input of a 2 input gate is 0 if and only if its inputs are unequal. It is true for,

   a) XNOR b) AND

   c) NOR d) NAND

7. The output of Boolean Function A + AB is,

   a) B b) O

c) A d) A + B

8. How many clock pulses are required to enter a byte of data serially into an 8 bit shift register?

a) 16 b) 8

c) 4 d) 1

9. A 10 MHz clock frequency is applied to a cascaded counter consisting of a modulus- 5 counters, a modulus- 8 counters, and two modulus- 10 counters. The lowest output frequency possible is,

a) 10 KHz b) 2.5 KHz

c) 5 KHz d) 25 KHz

10. If an S-R latch has a 1 on the S input and O on the R input and then the S input goes to O, the latch will be,

a) set b) reset

c) toggle d) clear

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Semester: I^st^

Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

11. What is digital System? Write down the advantage and limitation of digital System. [1 + 2 + 2]

12. Why NAND and NOR gates are called Universal Gates? Implement AND, OR and NOT Gates using NAND and NOR gates. [1 + 2 + 2]

13. Simplify using K - map and draw the logical diagram.

$$F = \overline{w}xz + \overline{w}yz + \overline{x}y\overline{z} + wx\overline{y}z + wy\overline{z}$$ [4 + 1]

14. Explain half adder. Implement full adder using two half adder and OR gate. [1 + 4]

15. Draw a logic diagram, graphical symbol, characteristic table, characteristic equation and excitation table of S.R flip flop. [1 + 1 + 1 + 1 + 1]

16. Design a MOD - 5 counter using J.K flip flop. [5]

17. Define shift Register. Explain the working principle of SISO shift register. [1 + 4]

Group C

Attempt any TWO questions. **[2×10 = 20]**

18. a) What is decoder? Implement 5 × 32 decoder using 2 × 4 decoder. [1 + 4]

    b) If A = 20 and B = 7 convert them into binary and perform A–B using 2's complement method. [1 + 4]

19. Explain asynchronous counter. Explain the digital watch with suitable diagram. [2 + 8]

20. Design a 2 bit counter with J.K flip-flop which counts up when x = 1 and counts down when x = 0. [10]

SET - B

Tribhuvan University

Faculty of Humanities & Social Sciences

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2018

Bachelor in Computer Applications **Full Marks: 60**

Course Title: Digital Logic **Pass Marks: 24**

Code No: CACS 105 **Time: 3 hours**

Semester: Ist

Centre: **Symbol No:**

Candidates are required to answer the questions in their own words as far as possible.

Group A

Attempt all the questions. **10×1 = 10**

Circle (O) the correct answer.

2. Which one of the following is octal equivalent of $(110001.0010)_2$?

   a) 45.10   b) 61.10

   c) 61.01   d) 62.10

2. Which one of the following is 1's complement of $(1001.001)_2$?

a) 0110.101 b) 1101.110

c) 0110.110 d) 1001.101

3. Which one of the following is the equivalent gray code of 1111?

a) 1001 b) 1101

c) 1000 d) 1010

4. If a 3- input NOR gate has eight input possibilities, how many of those possibilities will result in a high output?

a) 2 b) 1

c) 6 d) 8

5. A binary parallel adder producer the arithmetic sum in,

a) Parallel b) Serial

c) Sequence d) Both a and b

6. A basic S-R flip-flop can be constructed by cross-coupling of which logic gates?

a) AND or NOR b) NAND or NOR

c) XOR or XNor d) AND or OR

7. A J-K flip-flop is in a "no change" condition when ....

a) J = 1, K = 1 b) J = 1, K = 0

c) J = 0, K = 1 d) J = 0, K = 0

8. When two counters are cascaded, the overall MOD number is equal to the .... of their individual MOD number.

a) log b) reciprocal

c) product d) sum

9. Which segments of a seven–segment display would be required to be active to display the decimal digit 2?

a) a, b, d, e and g b) a, b, c, d and g

c) a, c, d, f and g d) a, b, c, d, e and f

10. In a parallel in/parallel out shift register, $D_0 = 1$, $D_1 = 1$, $D_2 = 1$ and $D_3 = 0$. After a three clock pulses, the data outputs are ....

a) 1110 b) 0001

c) 1100 d) 1000

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Bachelor in Computer Applications | **Full Marks: 60**
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Candidates are required to answer the questions in their own words as far as possible.

Group B

Attempt any SIX questions. **[6×5 = 30]**

11. Subtract: 675.6 – 456.4 using both 10's and 9's complement. [5]

12. What is university logic gate? Realize NAND and NOR as an universal logic gates. [1 + 2 + 2]

13. Simplify (using K- map) the given Boolean function F in both SOP and POS using don't care conditions

    A: $B'CD' + A'BC'D$

    $F = B'C'D' + BCD' + ABCD'$ [2 + 3]

14. Define encoder: Draw logic diagram and truth table of octal - to - binary encoder. [1 + 4]

15. What is D flip-flop? Explain clocked RS flip-flop with its logic diagram and truth table. [1 + 4]

16. Design MOD - 5 counter with state and timing diagram. [2 + 1 + 2]

17. Design a 4 - bit serial into parallel- out shift register with timing diagram. [3 + 2]

Group C

Attempt any TWO questions. **[2×10 = 20]**

18. Write difference between PLA and PAL. Design a PLA circuit with given functions.

    F1 (A, B, C) = ☒ (2, 3, 5)

    F2 (A, B, C) = ☒ (0, 4, 5, 7). Design PLA program table also. [3 + 7]

19. Define D flip-flop. Design a Master-slave flip-flop by using JK flip-flop along with its circuit diagram and truth table. [2 + 8]

20. Write down the difference between asynchronous and synchronous counter. Design a 4- bit binary ripple counter along with its circuit, state and timing diagram. [3 + 7]